

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims:

Claims:

1. (Canceled)
2. (Canceled)
3. (Canceled)
4. (Canceled)
5. (New) An integrated circuit comprising;

a test circuit that generates deterministic test vectors;

an application circuit coupled to receive and process the deterministic test vectors to produce output signals;

a logic gate coupled to receive the output signals and block X signal portions of the output signals in response to a first signal and output the remainder of the output signals;

and

a signature register coupled to receive the remainder of the output signals and generate a signature.
6. (New) The integrated circuit of claim 5 wherein the X signal comprises an ambiguous signal.
7. (New) The integrated circuit of claim 6 wherein the X signal is ambiguous due to influence by a circuit element in the application circuit which exhibits a storage property.

8. (New) The integrated circuit of claim 6 wherein the X signal is ambiguous due to influence by a circuit element in the application circuit which exhibits an analog behavior.
9. (New) The integrated circuit of claim 5 wherein the test circuit comprises
a test pattern generator for generating pseudorandom test patterns; and
a second logic gate for receiving the pseudorandom test patterns and modifying the pseudorandom test patterns into a deterministic test patterns in response to a second signal.
10. (New) The integrated circuit of claim 9 wherein the second signal is received from a source external to the integrated circuit.
11. (New) The integrated circuit of claim 9 wherein the test pattern generator is a linear feedback shift register.
12. (New) The integrated circuit of claim 5 wherein the first signal is received from a source external to the integrated circuit.
13. (New) An integrated circuit comprising;
means for generating deterministic test vectors;
means for receiving and processing the deterministic test vectors to produce an output signal;
means for receiving the output signals and a first signal and blocking X signal portions of the output signals in response to the first signal and outputting the remainder of the output signals; and
means for receiving the remainder of the output signals and generating a signature.
14. (New) The integrated circuit of claim 13 wherein the signature indicates if the application circuit is operating correctly.

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15. (New) The integrated circuit of claim 13 wherein the X signal comprises an ambiguous signal.
16. (New) The integrated circuit of claim 15 wherein the X signal is ambiguous due to influence by a circuit element in the application circuit which exhibits a storage property.
17. (New) The integrated circuit of claim 15 wherein the X signal is ambiguous due to influence by a circuit element in the application circuit which exhibits an analog behavior.